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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/822,166	03/30/2001	Ritesh Saraf	03226.082001;P5751	6279

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EXAMINER	
DOOLEY, MATTHEW C	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 06/10/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	09/822,166	SARAF, RITESH	
	Examiner	Art Unit	
	Matthew C. Dooley	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-13,15,17 and 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-13,15,17 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The informal drawings are of sufficient quality for examination purposes. However, new formal drawings will be required if and when the application is put in condition for allowance.

Response to Amendment

Claim Rejections - 35 USC § 102

2, The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3,5-13, 15, 17-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsunaga et al., U.S. 6,150,861.

As per claim 1:

Matsunaga teaches to flip-flop (f-f) circuitry that includes a data input control stage that selectively controls a value on a data node that is coupled to the master stage and the slave stage and a scan input control stage that selectively controls a value on a scan node that is coupled to the master stage (Fig.2). Moreover, Matsunaga teaches to one of the scan and data nodes being held constant when the other of the scan and data nodes is active (Abstract).

As per claim 2:

Matsunaga teaches to f-f circuitry wherein the data input control stage inputs a data input signal and a scan enable signal, and wherein the data input control stage resides on the topmost end of the f-f circuit (Fig.1,2).

As per claim 3:

Matsunaga teaches to f-f circuitry wherein the scan input control stage inputs a scan input signal and a scan enable signal, wherein the scan input control stage resides on the bottommost end of the f-f circuit (Fig.1,2).

As per claim 5:

Matsunaga teaches to a scan node that is active during the scan mode (Col.2: 35-36).

As per claim 6:

Matsunaga teaches to the scan node being pulled to a second value when the f-f is in normal mode, and wherein the data node is active during normal mode (Col.2: 33-42).

As per claim 7:

Matsunaga teaches to the master stage passing a value to the slave stage based on the scan and data node values (Fig.2; Col.3: 15-16).

As per claim 8:

Matsunaga teaches to delayed and inverted clock signals to the data and scan input control stages and the master and slave stages (Fig.1, 2; Col. 3: 30-45).

As per claim 9:

Matsunaga teaches to a data input signal that selectively controls the value on the data node dependent on the clock input control stage (Col.3: 30-54).

As per claim 10:

Matsunaga teaches to a data input signal that selectively controls the value on the scan node dependent on the clock input control stage (Col.3: 30-54).

As per claim 11:

Matsunaga teaches to the master stage selectively passing a value to the slave stage dependent on the data and scan nodes and the clock input control stage (Fig.2: Col.3: 30-54).

As per claim 12:

Matsunaga teaches to the slave stage selectively controlling the output value of the f-f dependent on the data node and the clock input control stage (Fig.2: Col.3: 30-54).

As per claim 13:

Matsunaga teaches to f-f methodology that includes selectively controlling a value on a data node dependent on a data input control stage and the clock input control stage, wherein the data node is coupled to the master and slave stage, selectively controlling a value on a scan node dependent on a scan input control stage and the clock input control stage, wherein the scan node is coupled to the master stage, selectively controlling the slave stage dependent on the master stage and the clock input control stage, and selectively generating an output of the f-f dependent on the slave stage (Fig.1, 2; Col.2: 33-67; Col.3: 30-54). Moreover, Matsunaga teaches to one of the scan and data nodes being held constant when the other of the scan and data nodes is active (Abstract).

As per claim 15:

Matsunaga teaches to a scan node that is active during the scan mode (Col.2: 35-36).

As per claim 17:

Matsunaga teaches to the data node being active during normal mode (Col.2: 33-42).

As per claim 18:

Matsunaga teaches inputting a clock signal to the clock input control stage and generating delayed and inverted clock signals (Fig.1, 2; Col. 3: 30-45).

Response to Arguments

4. Applicant's arguments filed 03/23/04 arguing the allowability of newly amended independent claims 1 and 13 have been fully considered but they are not persuasive. The Applicant has argued that amendments to claims 1 and 13 make the aforementioned claims allowable over Matsunaga. The Examiner respectfully disagrees. Matsunaga anticipates holding one of the data and scan nodes constant while the other is active, specifically calling for N1 to track an input signal during a first portion of the clock signal, and to remain constant during the second portion of the clock signal, while N2 tracks the output signal during the second portion of the clock signal, while remaining constant during the first portion of the clock signal (Abstract). As such, the arguments that the amendments to claims 1 and 13 are not persuasive. Moreover, as the remaining dependent claims were argued to be allowable for further limiting claims 1 and 13, they too remain rejected.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Dooley whose telephone number is (703) 306-5538. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matt Dooley

Matthew Dooley
Examiner AU 2133
06/02/04

CHRISTINE T. TU
Primary Examiner